

What is claimed is:

1 1. A floating gate having improved coupling ratio,
2 comprising:

3 a semiconductor substrate;

4 a tunneling dielectric layer formed on the
5 semiconductor substrate;

6 a conductive layer, formed on the tunneling
7 dielectric layer; and

8 a plurality of conductive spacers, formed on the
9 sidewalls of the conductive layer, and the tops
10 of the conductive spacers level with the
11 surface of the conductive layer, with the
12 conductive spacers and the conductive layer
13 forming the floating gate.

1 2. The floating gate as claimed in claim 1,
2 further comprising two neighboring shallow trench
3 isolation structures, and the tunneling dielectric layer
4 located between the two shallow trench isolation
5 structures.

1 3. The floating gate as claimed in claim 1,
2 wherein the conductive layer is doped polysilicon, doped
3 amorphous silicon, undoped polysilicon, undoped amorphous
4 silicon or polycide.

1 4. The floating gate as claimed in claim 1,
2 wherein the conductive spacers are doped polysilicon,
3 doped amorphous silicon, undoped polysilicon, undoped
4 amorphous silicon or polycide.

1 5. The floating gate as claimed in claim 1,
2 wherein the tunneling dielectric layer is oxide or
3 oxynitride.

1 6. The floating gate as claimed in claim 1,
2 wherein the insulation layer is nitride.

1 7. A floating gate having improved coupling ratio,
2 comprising:

3 a semiconductor substrate;

4 a tunneling dielectric layer formed on the
5 semiconductor substrate;

6 a conductive layer, formed on the tunneling
7 dielectric layer;

8 a pair of shallow trench isolation formed oppositely
9 adjacent to the conductive layer, wherein the
10 shallow trench isolation is lower than the top
11 surface of the conducting layer; and

12 a plurality of conductive spacers, formed on the
13 sidewalls of the conductive layer and overlying
14 the shallow trench isolation, and the tops of
15 the conductive spacers level with the surface
16 of the conductive layer, with the conductive
17 spacers and the conductive layer forming the
18 floating gate.

1 8. The floating gate as claimed in claim 7,
2 wherein the conductive layer is doped polysilicon, doped
3 amorphous silicon, undoped polysilicon, undoped amorphous
4 silicon or polycide.

1 9. The floating gate as claimed in claim 7,
2 wherein the conductive spacers are doped polysilicon,
3 doped amorphous silicon, undoped polysilicon, undoped
4 amorphous silicon or polycide.

1 10. The floating gate as claimed in claim 7,
2 wherein the tunneling dielectric layer is oxide or
3 oxynitride.

1 11. The floating gate as claimed in claim 7,
2 wherein the shallow trench isolation is an oxide layer.